

*Sub cancel*  
a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions,

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

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*Sub F1*  
6. (Thrice Amended) A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said first source and drain regions;

*Contd*  
D2 wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions, wherein said semiconductor layer of said p-channel TFT has no LDD regions.

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D3 11. (Thrice Amended) A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a pair of LDD regions and first source and drain regions;

wherein said first gate electrode partially overlaps said pair of LDD regions, and said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film interposed therebetween, said second semiconductor layer comprising a second channel formation region and second source and drain regions being in contact with said second channel formation region,

13 wherein <sup>said</sup> second gate electrode partially overlaps said second source and drain regions, and

wherein a wiring is connected to at least one of said second source and drain regions.

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*D3*

14. (Thrice Amended) A goggle type display device having a CMOS circuit comprising an

n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions,

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

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*D4*

19. (Thrice Amended) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

*Cont'd*  
a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said first source and drain regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions,

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

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*Subj 2*  
24. (Thrice Amended) A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a pair of LDD regions and first source and drain regions;

wherein said first gate electrode partially overlaps said pair of LDD regions, and  
said p-channel TFT comprising: